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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,248	06/26/2003	Oliver Kiehl	1115747-0005//2002P50545U	7758

25962 7590 07/08/2004

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,248	KIEHL ET AL.	
	Examin r	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/26/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The specification is objected because it fails to teach "the gate terminal of the second transistor coupled to the gate terminal of the first transistor, the gate terminals of the first and second transistors coupled to the first non-gate terminal of the first and second transistors", claim 19, and "the gate is directly connected to the drain", claim 40.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "the gate terminals of the first transistor and second transistor coupled together" (claim 19) and "the gate is directly connected to the drain" (claim 40) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted

by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 19-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 19 recites "the gate terminal of the second transistor coupled to the gate terminal of the first transistor, the gate terminals of the first and second transistors coupled to the first non-gate terminal of the first and second transistors". The current circuit will not work properly since the gate of the first and second transistors are also receiving clock signals as described in the specification.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 19-21 and 30-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 19 is misdescritive to recite "the gate terminal of the second transistor coupled to the gate terminal of the first transistor, the gate terminals of the first and second transistors

coupled to the first non-gate terminal of the first and second transistors" the drawings do not shows that the gates of the first and second transistors are coupled together.

Claims 20-21 are rejected as including the indefiniteness of claim 19.

Claim 30 is indefinite because there is no antecedent basis for the limitation "the transistor".

Claims 31 and 32 are rejected as including the indefiniteness of claim 30.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-5, 9-13, 15-39 and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Yung et al. (USP 5525927).

As to claim 1, Yung et al. discloses in figure 3 a current source (M1, M0, M10) for use in an integrated circuit providing an extended voltage range, comprising: a first transistor (M10) having first and second non-gate terminals (drain and source); a second transistor (M9) having first and second non-gate terminals (drain and source), the first non-gate terminal coupled to the first non-gate terminal of the first transistor; and a bias generator (M1) having a non-gate terminal (drain) coupled to the second non-gate terminals of the first and second transistors, the bias generator further having a gate terminal coupled to the first non-gate terminals of the first and second transistors.

As to claim 2, figure 3 shows the voltage range comprises a common mode range.

As to claim 3, figure 3 shows the second non-gate terminals of the first and second transistors comprise sources.

As to claim 4, figure 3 shows at least one of the first transistor, second transistor, and bias generator comprises an NMOS transistor.

As to claim 5, figure 3 shows the bias generator comprises a transistor.

As to claim 9, figure 3 shows the first and second transistors are coupled in parallel.

As to claim 10, figure 3 shows a method of extending a voltage range of a current source for differential amplifiers and comparators in an integrated circuit, the method comprising the steps of: providing a first transistor (M10), a second transistor (M9), and a third transistor (M1), the first and second transistors each having a drain and a source, the third transistor having a gate and a drain; connecting the drain of the first transistor to the drain of the second transistor; connecting the source of the first transistor to the source of the second transistor; connecting the gate of the third transistor to the drains of the first and second transistors; and connecting the drain of the third transistor to the sources of the first and second transistors.

As to claim 11, figure 3 shows the voltage range comprises a common-mode range.

As to claim 12, figure 3 shows a current source for use in an integrated circuit providing an extended voltage range, comprising: a voltage source (VDD); a current source (Ib) having a positive and negative terminal, wherein the positive terminal is connected to the voltage source; a first NMOS transistor (M10) having a source terminal and drain terminal, the drain terminal connected to the negative terminal of the current source; a second NMOS transistor (M9) having a source terminal and drain terminal, the drain terminal of the second NMOS transistor connected to the drain terminal of the first NMOS transistor, the source terminal of the second

NMOS transistor connected to the source terminal of the first NMOS transistor; and a third NMOS transistor (M1) having a gate terminal and drain terminal, the drain terminal of the third NMOS transistor connected to the source terminals of the first and second NMOS transistors, the gate terminal of the third NMOS transistor connected to the drains of the first and second NMOS transistors.

As to claim 13, figure 3 shows the voltage range comprises a common-mode range.

As to claim 15, figure 3 shows a current source for use in an integrated circuit providing an extended common mode range, comprising: means (M9, M10) for regulating a gate-to-source voltage using a differential pair; and coupled to the regulating means, a current driving transistor (M1).

As to claim 16, figure 3 shows a constant current source for use in an integrated circuit extending a voltage range, comprising: a first transistor (M10) having first and second non-gate terminals; a second transistor (M9) having first and second non-gate terminals, the first non-gate terminal coupled to the first non-gate terminal of the first transistor; a bias generator (M1) having a non-gate terminal coupled to the second non-gate terminals of the first and second transistors, the bias generator further having a gate terminal coupled to the first non-gate terminals of the first and second transistors; and a fully differential receiver (M2, M5m M6) connected to at least one of the first non-gate terminals of the first and second transistor.

As to claim 17, figure 3 shows the voltage range comprises a common-mode range.

As to claim 18, figure 3 shows the first and second transistors are coupled in parallel.

Insofar as understood, claims 19-21 recite similar limitations with claims 16-18. Therefore they are rejected for the same reasons.

As to claim 22, figure 3 shows a constant current source for use in an integrated circuit to extend a voltage range of a differential amplifier circuit, comprising: a first transistor (M10) having first and second non-gate terminals; a second transistor (M9) having first and second non-gate terminals, the first non-gate terminal coupled to the first non-gate terminal of the first transistor; a bias generator (M1) having a non-gate terminal coupled to the second non-gate terminals of the first and second transistor, the bias generator further having a gate terminal coupled to the: first non-gate terminals of the first and second transistors; and a differential amplifier (M2, M5-M8) coupled to at least one of the first non-gate terminals of the first and second transistors.

As to claim 23, figure 3 shows the voltage range comprises a common-mode range.

As to claim 24, figure 3 shows the first and second transistors are coupled in parallel.

As to claim 25, figure 3 shows a method for extending a voltage range of a current source in an integrated circuit, the method comprising the steps of: providing a first transistor (M10) and a second transistor (M1), the first transistor having a drain terminal and the second transistor having a gate terminal; measuring a drain terminal voltage of the first transistor; and, based on the drain terminal voltage, regulating a gate terminal voltage of the second transistor.

As to claim 26, figure 3 shows the voltage range comprises a common-mode range.

As to claim 27, figure 3 shows a third transistor (M9) having a drain terminal; measuring a drain terminal voltage of the third transistor; and based on the drain terminal voltage, regulating a gate terminal voltage of the second transistor.

As to claim 28, figure 3 shows a current source for use in an integrated circuit providing an extended voltage range, comprising: a circuit (M1) for measuring a drain voltage using a

differential pair (M9, M10); and a circuit for regulating a gate voltage based on the drain voltage measured at the differential pair.

As to claim 29, figure 3 shows the voltage range comprises a common-mode range.

As to claim 30, figure 3 shows a method of extending a voltage range of a current source in an integrated circuit, the method comprising the steps of: providing a constant current source in a saturation region of a transistor; and maintaining the constant current if the transistor (M1) exits the saturation region.

As to claim 31, figure 3 shows the constant current is maintained by increasing the gate voltage of the transistor when the transistor leaves the saturation region.

As to claim 32, figure 3 shows the voltage range comprises a common-mode range.

As to claim 33, figure 3 shows a method for extending a voltage range of a current source in an integrated circuit, the method comprising the steps of: measuring a drain voltage (of M10) of a transistor (M10); and regulating a gate voltage (of M1) based on the drain voltage of that transistor.

As to claim 34, figure 3 shows the gate voltage is regulated such that the current remains constant even if the transistor is not in saturation.

As to claim 35, figure 3 shows a method for extending a voltage range of a current source in an integrated circuit, the method comprising the steps of: measuring a drain voltage using a differential pair (M10, M9); and regulating a gate voltage (of M1) based on the drain voltage measured at the differential pair.

As to claim 36, figure 3 shows the voltage range comprises a common-mode range.

As to claim 37, figure 3 shows a current source for use in an integrated circuit having an extended voltage range comprising: a transistor (M1) having a drain characterized by a voltage; and a gate having a voltage that is reactive to the voltage of the drain.

As to claim 38, figure 3 shows the gate voltage is regulated based on the drain voltage.

As to claim 39, figure 3 shows the gate is not directly coupled to the drain.

As to claim 41, figure 3 shows the voltage range comprises a common-mode range.

8. Claims 37 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicant admitted prior art figure 3c.

As to claim 37, figure 3 shows a current source for use in an integrated circuit having an extended voltage range comprising: a transistor (transistor that coupled to node 350) having a drain characterized by a voltage; and a gate having a voltage that is reactive to the voltage of the drain.

As to claim 40, figure 3c shows the gate is directly coupled to the drain.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims are rejected under 35 U.S.C. 103(a) as being unpatentable over Yung et al. (USP 5525927).

As to claims 6 and 14, Yung et al.'s figure 3 shows all limitations of the claim except for a capacitor coupled to the first non-gate terminals of the first and second transistors. However, it

is notoriously well known in the art that capacitor is for filtering and stabilizing biasing voltage signal. Therefore, it would have been obvious to one having ordinary skill in the art to add a capacitor coupled to the output of Yung et al.'s current source for the purpose of stabilizing the output voltage.

As to claims 7 and 8, the prior art fails to teach the capacitor has capacitance less than or equal to approximately 1 pF or 1fF. However, the selection of the capacitor to be less than or equal to approximately 1 pF or 1fF is seen as an obvious design preference dependent upon particular environment of use to ensure optimum performance.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The reference is cited as interest because it shows a circuit analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Patent Examiner

July 6, 2004